ABSTRACT OF THE DISCLOSURE

It is an object to obtain a semiconductor device capable of minimizing an increase in a gate capacity without adversely influencing an operation characteristic and a method of manufacturing the semiconductor device. A first trench (7) and a second trench (11) are formed to reach an upper layer portion of an N^- layer (3) through a P base layer (5) and an N layer (4), respectively. In this case, a predetermined number of second trenches (11) are formed between the first trenches (7) and (7). The first trench (7) is provided adjacently to an N^+ emitter region (6) and has a gate electrode (9) formed therein. The second trench (11) has a polysilicon region (15) formed therein. The second trench (11) is different from the first trench (7) in that the N^+ emitter region (6) is not formed in a vicinal region and the gate electrode (9) is not formed therein. A trench space between the first trench (7) and the second trench (11) which are provided adjacently to each other is set to be such a distance as not to reduce a breakdown voltage. An emitter electrode (12) is directly formed on an almost whole surface of a base region (5).